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A Review on Model-Free Time-Delay Compensation Techniques

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Abstract:
Recent advancements in digital signal processing technology have led to the use of digital microprocessors for controlling grid-connected inverters. However, digital realization suffers from phase lag caused by temporal delays. This phase lag tests the inverter controller's stability and durability. This work provides a detailed evaluation of time-delay compensation approaches for both model-free (MF) and model-based (MB) inverter controllers in grid connections. MF approaches mostly use proportional-integral and proportional resonance controllers, with some strategies for reducing time delay. Meanwhile, for MB, this study describes the most often utilized control strategies, including the Smith predictor, modified Smith predictor. Several comparable strategies from the literature that have been used to reduce delays are fully summarized, and significant concerns concerning the MF and MB procedures are also addressed. Finally, this work gives a hypothesis on which approach is currently preferable and proposes a hybrid technique combining the MF and MB procedures to provide readers with a path for future research.

Keywords: *Model-Free, Time Delay, Compensation Techniques, Digital Signal Processing.*

I. INTRODUCTION

In recent times, conventional power systems are experiencing an evolutional shift in the traditional way they work as a consequence of the growth in energy demand in the globe. There fore, in response to increasing worldwide need, networks need to be lib eralised for new sources of energy, such as solar and wind, to be included. These renewable energy resources have the potential of generating an exceptional contribution of electricity to the main grid if harnessed and exploited completely within a controlled setting. Distributed generation (DG) is becoming a com monapproach to fulfill this need, where DG systems are sys tematically linked using a power electronic equipment called grid-connected inverters to create what is termed the microgrid.

Theidea ofputting the individual DG together is to have system flexibility, which provides system optimisation, reliability, protec tion, integrity, security and power-quality control. New and strict rules for safe operating, power quality, and islanding protection are described in [2] since the interacting devices have certain difficulties with the grid, particularly when the grid is poor [1]. Therefore, these interconnection issues have garnered a lot of attention lately, and more research has been done as a result of the adoption of real-time-based controllers that can implement complex and sophisticated control algorithms as well as the discovery of power electronic devices that can handle high power and switch very quickly [3]. There are several disadvantages to using real-time-based controllers, including a delay in the control loop and a delay when switching between islanded and grid-connected modes.

A physical system's ability to respond to an applied force with a delayed impact is known as time-delay [4]. There is always a propagation delay along the channel when sending energy or a control signal from one location to another. The sent signal's speed and the kind of material it is traveling through are related to the propagation delay's magnitude. Thus, a lengthy delay in the digital control loop of the inverter or during the switch between grid-connected and islanded mode complicates the design and execution of the controller and exacerbates frequency and voltage aberrations. On the other hand, a brief delay may be readily managed using a variety of compensatory strategies.

A voltage, current, or direct power controller, or a combination of these controllers in a cascaded loop with an inner-loop or outer-loop topology, may be used in grid-connected inverters with LCL filters. Many studies use inner current control to provide precise current tracking, sufficient control bandwidth, and quick transient response. In contrast, the current controller is used in voltage source inverters (VSI) to enable the inverter to function as a current amplifier within the current loop bandwidth [5]. On the other hand, in the outer-loop structure, the voltage controller is used to reject disturbances from the grid and input sources and to guarantee power flow in the system. However, time-delay in the control loop, particularly in digital

implementation, limits the existing controller's control bandwidth.
Additionally, because of advancements in digital signal processing technology, digital microprocessors are used to regulate grid-connected inverters [6]. High dependability, more control flexibility, and quick reprogrammability are some benefits of the digital realization over the analog control. There are a few issues with this digital implementation, though, the most significant of which is the phase lag that the time delay causes in the control loop.
Using additional control loops will increase this delay even further.

Understanding the main reasons why time-delay occurs in the control loop of a grid-connected inverter is essential before going over some of the often utilized time-delay compensation strategies. The zero-order hold effect of digital pulse-width modulation [8], controller calculation time [7], and sampling and updating of voltage and current values for control purposes [9] are the primary causes of time delays in digital controller implementation. As a result, attaining high performance seems to be quite challenging when the control loop has a large time delay. As a consequence, the controller has a lower control bandwidth, a higher overshoot (an inadequate phase margin), and a lower transient response (low-gain cross-over frequency).

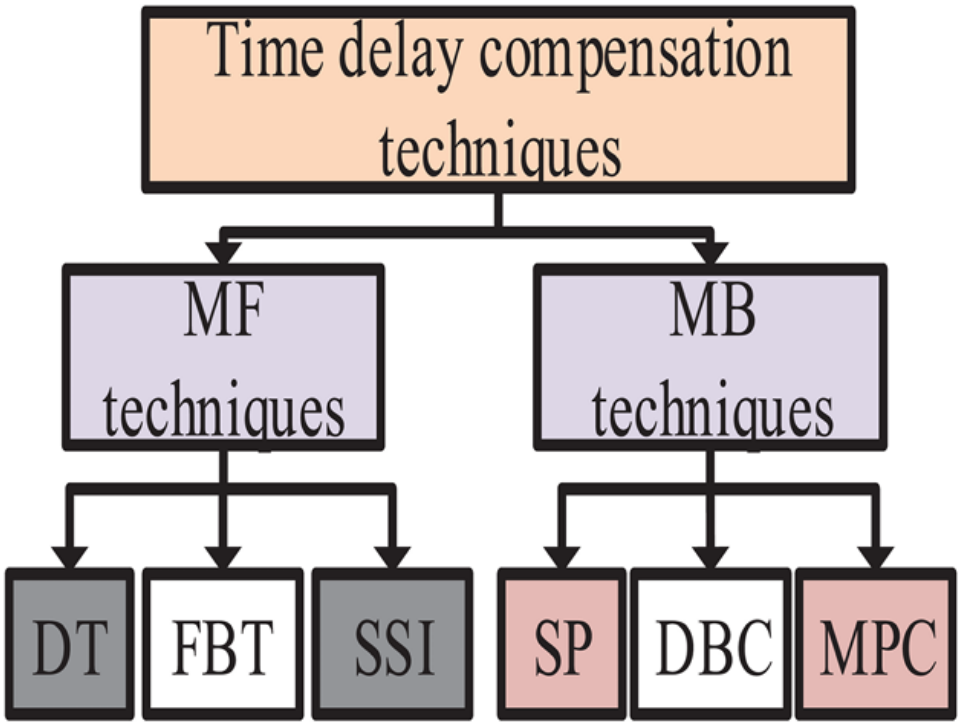
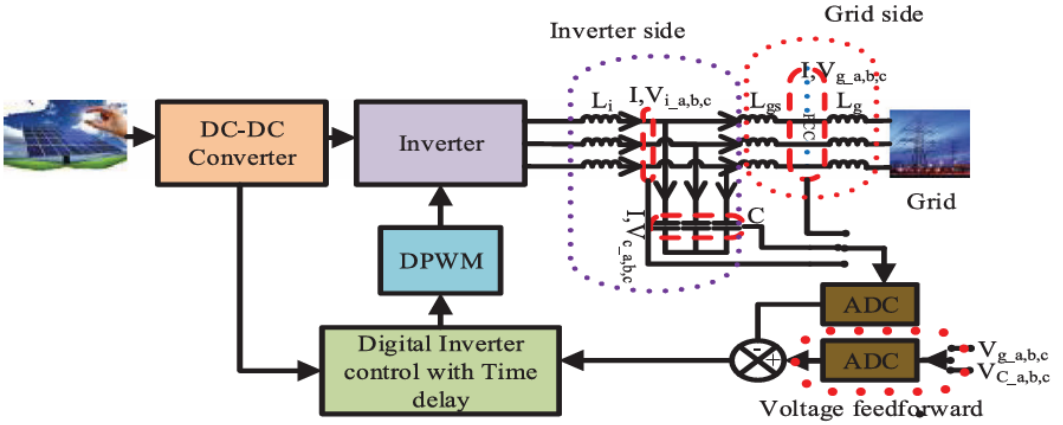


Fig 1 : Common time-delay compensation techniques for grid connected inverter

Additionally, this will worsen the controller's performance and lead to instability, to name a few of issues. Consequently, compensators are used to lessen or completely eradicate the delays in order to address these impacts. As shown in Figure 1, a variety of time-delay compensation strategies have been put out in the literature and may be categorized as either model-based (MB) or model-free (MF) strategies [6]. While MF approaches are less accurate but unaffected by the quality of the model, MB techniques are more accurate but sensitive to the precision of the system modeling. The Smith predictor (SP), modified Smith predictor (MSP), deadbeat controller (DBC), model predictive controller (MPC), and others are examples of MB time-delay compensation techniques. Conversely, MF approaches included the filter-based technique (FBT), the shifting the sampling instant (SSI) of the control variable, and the damping technique (DT) [6]. This paper's purpose is to draw attention to current issues and methods for decreasing the impact of time delay in the control loop of grid-connected inverters. It also suggests a path for future study on time delay reduction.
deadbeat controller (DBC), and model.

II. MODEL-FREETIME-DELAY

Since the LCL filter has the capability to reduce high frequency switching harmonics at the output of the inverter, it has been used in recent times to replace the standard L-type filter for grid-connected inverters. This is due to the fact that the LCL filter has these capabilities. On the other hand, this benefit does not come without a drawback, which is that it might lead to instability of the system when it is put into practice because of the zero impedance that occurs at the resonance frequency [10]. If the time-delay effect is taken into consideration inside the control loop of the inverter, then this weakness will become much more severe. Therefore, a great deal of work has been put out by a number of researchers in order to simultaneously address the oscillation issue of the LCL filter and minimize the time delay in the control loop. A presentation of the most often used MF strategies for time-delay compensation is going to take place in the subsequent subsections.



Note :$I,V_{i\_a,b,c}$, $I,V_{c\_a,b,c}$, $I,V_{g\_a,b,c}$: Point of measurement for the inverter side and grid side, DPWM: Digital pulse width modulation

Fig 2 : Schematicdiagramofagrid-connected inverter

III. TECHNIQUES

3.1 Damping techniques

The LCL filter's oscillation issue and the control loop's time delay are resolved by damping methods, which are separated into passive and active damping approaches. By adding a resistor in series with the filter inductor or capacitor, the passive damping approach suppresses the resonant peak and stabilizes the system. This method is easy to use and reasonably priced. Nevertheless, power loss, decreased filter efficacy, and a decline in system performance are all brought on by the additional resistor [11]. Consequently, these disadvantages reduce the acceptability of this damping strategy, particularly in a poor distribution grid. The active damping approach is an alternative to passive damping in which the oscillations are dampened and the time delay is compensated by using the observed state variables in place of a resistor. This method is further separated into two categories: grid-side active damping and inverter-side active damping.

According to [12–15], the inverter-side active damping approach uses feed-forward current or voltage state variables or single, double, or multi-loop feedback to create superior damping and reduce time-delay in the control loop. As shown in Figure 2, state variable measurements are performed on the filter capacitor or inductor at the inverter side. In the grid-side active damping technique, a single-, double-, or multi-loop grid current or voltage feedback or feed-forward is used, as shown in Figure 2, to dampen the oscillation in the system and to mitigate the time-delay. However, even though good results were reported from this technique, the single-loop technique cannot guarantee stability in the presence of disturbances; at the same time, there is a need to measure more than one state variable in the double- and multi-loop topologies, which has a cost impact, lowers reliability, and tends to increase the complexity of the controller [10, 11]. According to reports, the grid-side active damping approach makes the system intrinsically unstable [16]. As a result, a time delay is included into the control loop to attain stability. The authors used this technique in [10], and they claim that the time-delay addition stabilizes the system in an efficient manner. The system is unstable when the time-delay is outside of the specified range, however, since the stability described in [10] is only true for a certain range of time-delay. Grid-connected inverters that need a quick controller with little latency cannot use this approach.

3.2 Filter-based techniques

In this method of compensation, the measured state variables are sent into the controller by means of a filter. Alternatively, a filter may be positioned in the cascade with the primary controller or it may be linked to filter the voltage reference to the modulator. The filter is able to correct for the phase lag that is induced by the

time delay in any of the modes, and this approach was used in [14, 17–20]. This method was chosen because it does not need an extra sensor. There are, however, certain downsides associated with this approach, including the fact that it amplifies noise, that it is difficult to tune the filter parameters, that the filter is sensitive to fluctuations in the parameters, and that it is very sensitive to variations in the grid impedance.

3.3 Shiftingthe sampling instant of the control variable or PWM updating instant techniques

When using pulse width modulation (PWM), it is a standard practice to take a sample of the state variables in the middle of each and every turn-on or turn-off period. This way, the average value of variables such as inductor current, capacitor current or grid current is sampled, as shown in Figure 3(a), where ms is the single-update PWM wave, the single-update PWM wave ms(K −1)ofthe(K −1)th carrier cycle is loaded at the peak of the (K −1)th triangular carrier and the duty cycle is expressed as M (K) = ms (K −1), where ms(K −1) is the duty cycle calculated by sampling values at the peak of the (K − 1)th triangular carrier [20]. The three sample points that are included in a single update are as follows: ms(K), ms(K − 1), and ms(K −2). This is seen in Figure 3(a). On the other hand, there are five sample points, denoted as ms(K) toms(K −5), present in double-updating, as seen in Figure 3(b). Furthermore, it is shown in Figure 3(c) that there are nine sample points in multi-updating, ranging from milliseconds (K) to milliseconds (K - 9). However, single sampling and updating often results in a delay of one switching period, which has the effect of restricting the bandwidth available to the controller at the moment.

This one-switching period delay can be further reduced to half switching period by using the double-update mode, as shown in Figure 3(b). In this mode, the control variables are sampled twice, and the update is carried out at the peak and valley of the triangular carrier twice at the middle of the turn-on and turn-off time of the pulse width. One alternative is to use the double-update mode. In addition, a number of scholars suggested that moving the instant at which control variables are sampled closer to the duty cycle update instants might further contribute to the reduction of the time delay; this method has been implemented in [21–23]. When adopting this method, however, there is a possibility that the asynchronous sampling procedure may result in the presence of harmonics that are not desirable [6].

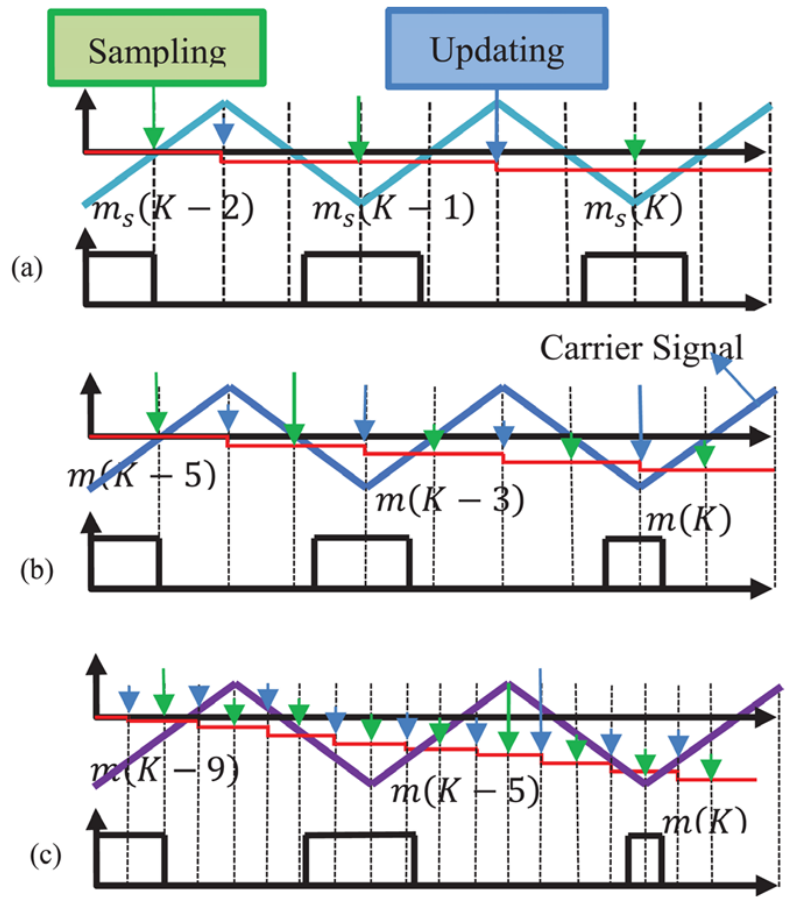


Fig 3 : (a)Singleupdating,(b)double updating and (c) multi-updating

However, despite the fact that the authors in [21] did adopt the method of sampling the control variables toward the duty cycle updating instants, they believed that the conventional sampling at the middle of the turn-on and turn-off time of the PWM has a greater tendency of reducing harmonics disturbances than the shifting toward the duty cycle updating instants. This was the conclusion that they came to. The sampling of the state control variables and the updating of the duty cycle many times during a single switching period is an additional method that may be used to further decrease the amount of time that is wasted. This is seen in Figure 3(c). It is a method that is known as the multi-sampling, multi-updating approach. This approach is suited for implementation on a field-programmable gate array (FPGA), as stated in reference.

IV. CONCLUSIONS

The purpose of this study is to provide a complete summary of the analytical contributions that were made by earlier research on time-delay compensation strategies in the control loop of grid-connected inverters. MF was found to be more adopted in this area of research due to its simplicity and average performance despite the challenges in terms of the stability of the system in both the inverter-side and grid-side topologies. This review is classified based on the dependency of the controller to the model of the system (MF and MB). Here I will discuss the differences between the two models. The robustness of these types of controllers is not guaranteed in the presence of disturbances or when the system is plugged into a weak grid. Despite the fact that numerous techniques were presented to compensate for time-delay and improve the stability of the system with a minimum number of sensors and less complexity, the robustness of these controllers is not guaranteed. After reviewing the model-based strategies, it was discovered that the Smith predictor and the modified Smith predictor were the first methods employed in balancing the impact of time-delays based on conventional PID controllers. This was discovered due to the fact that the Smith predictor was the first way applied.

This method is less relevant to grid-connected inverters due to the limitations of these controllers, which include the inability to handle time-varying signals and a low level of disturbance rejection. DBC, on the other hand, has lately gained popularity due to the fact that it is capable of quick current monitoring, zero steady-state error, time-delay compensation, and disturbance rejection. This approach is divided into two categories, according to the findings of this article, depending on whether or not the time delay impact is taken into consideration throughout the controller design process. As a result of the examination of research works that investigated the impact of time delay, it was discovered that a significant number of research works assumed that the DC-link voltage and grid voltage remained constant. Furthermore, the outer loop was not included into the controller design.

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